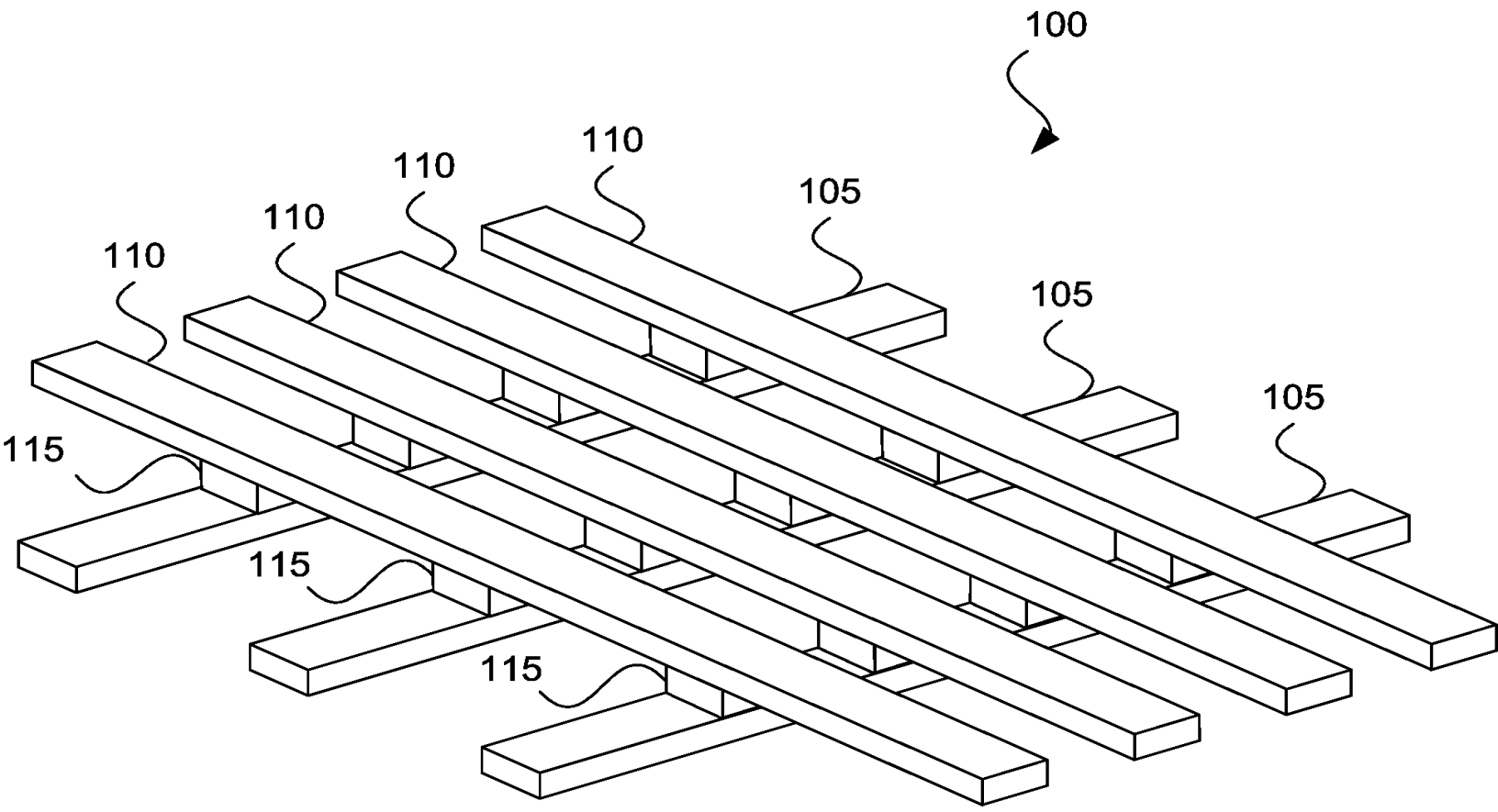
100
110
110
110
110
105
105
105
115
115
115

FIG. 1A

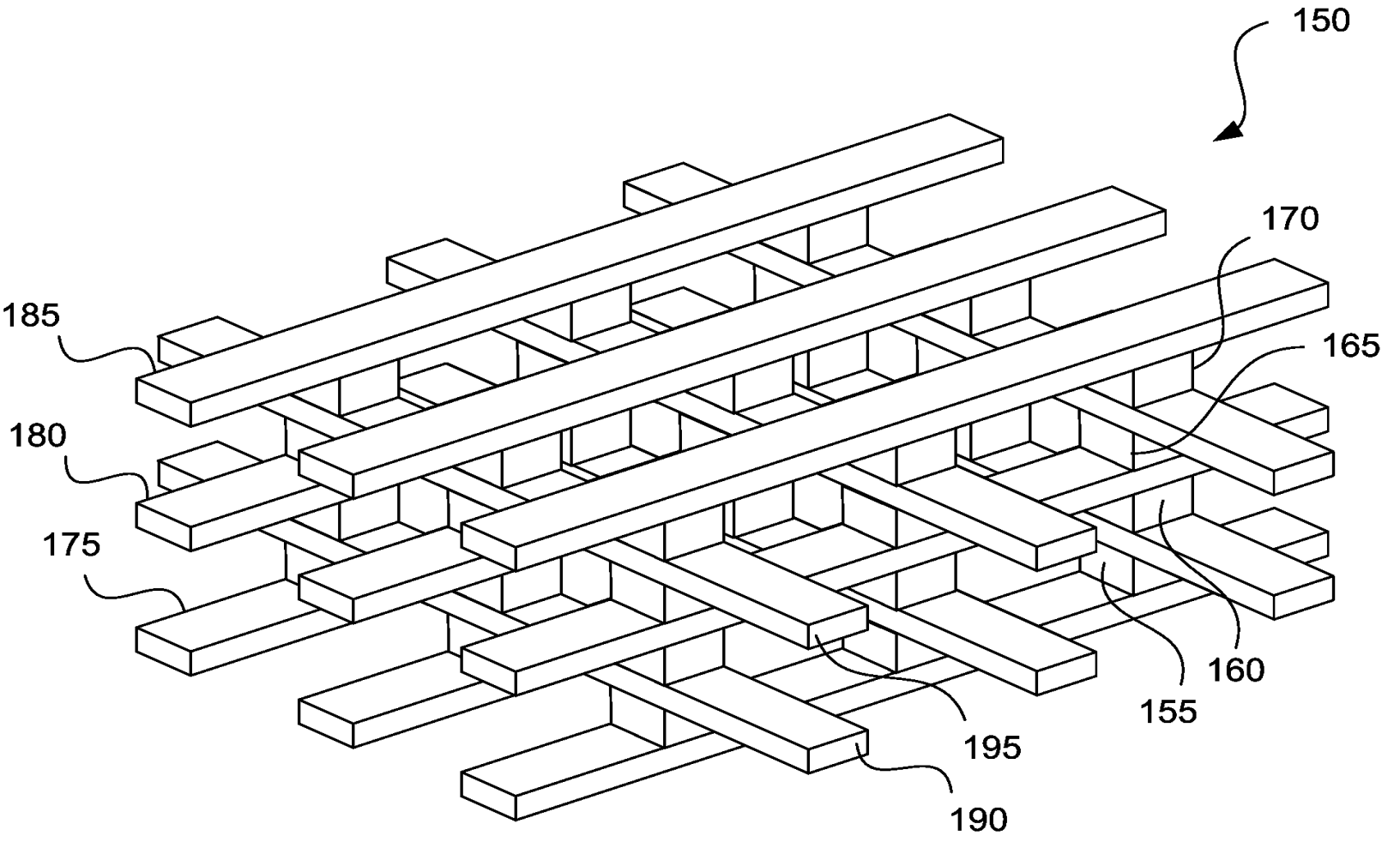
150
170
185
165
180
175
160
155
195
190

FIG. 1B

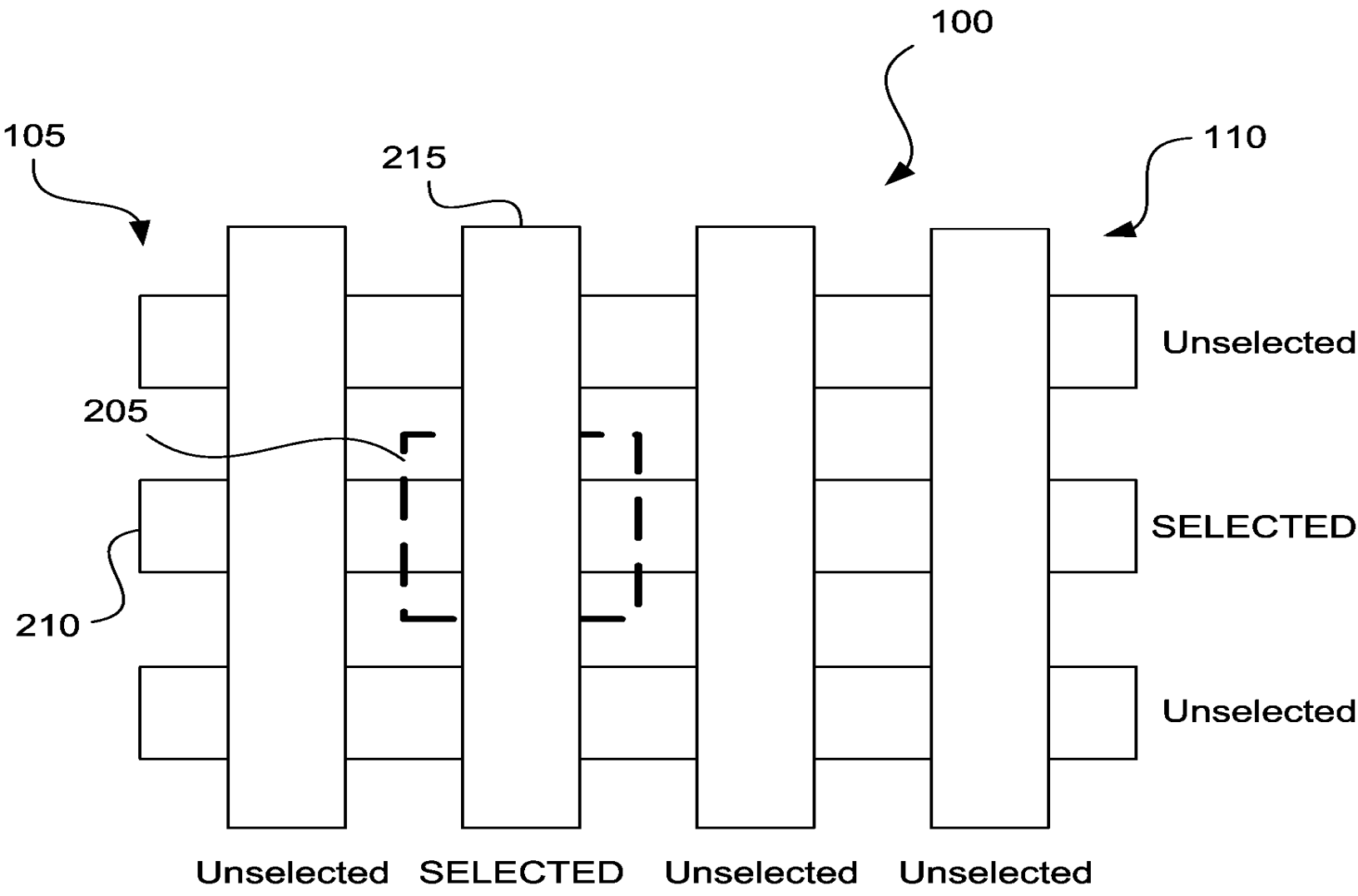
100
105
215
110
Unselected
205
SELECTED
210
Unselected
Unselected
SELECTED
Unselected
Unselected

FIG. 2A

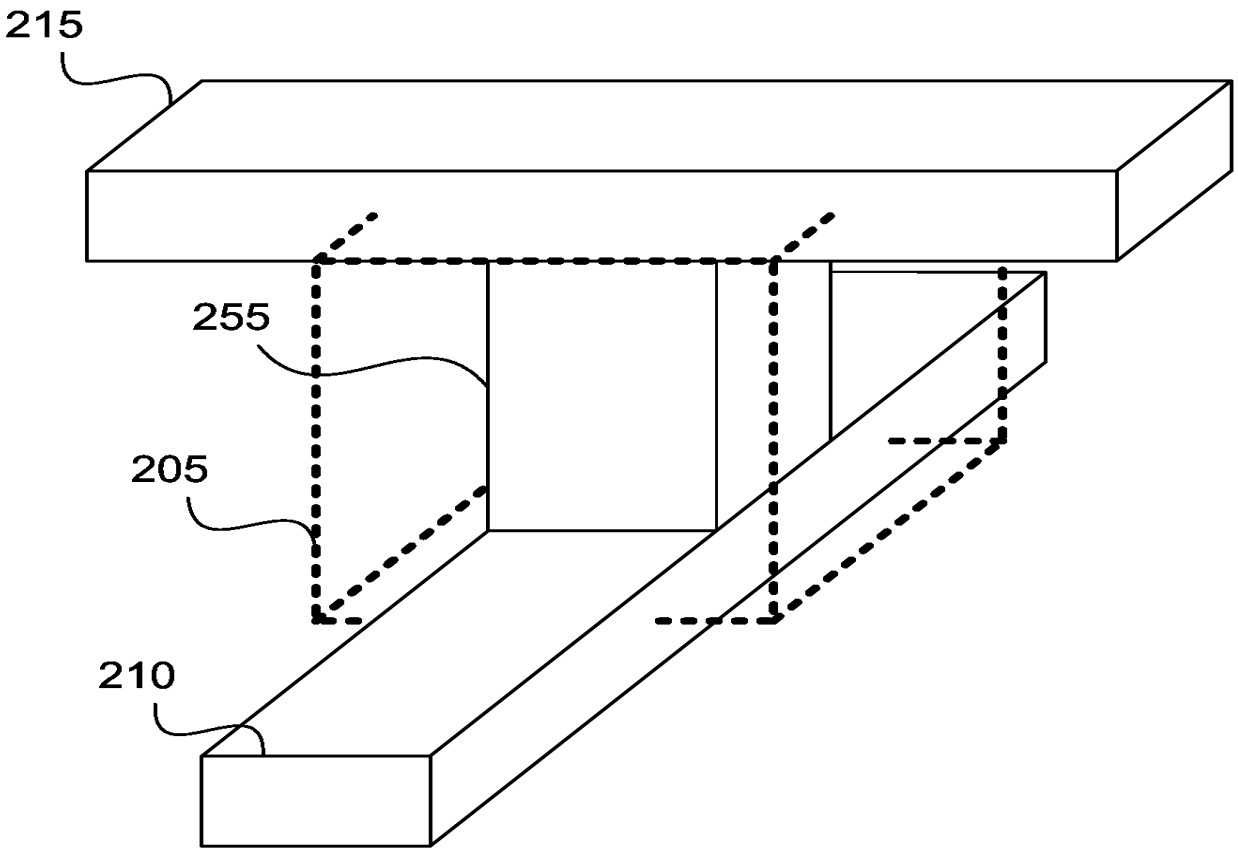
215
255
205
210

FIG. 2B

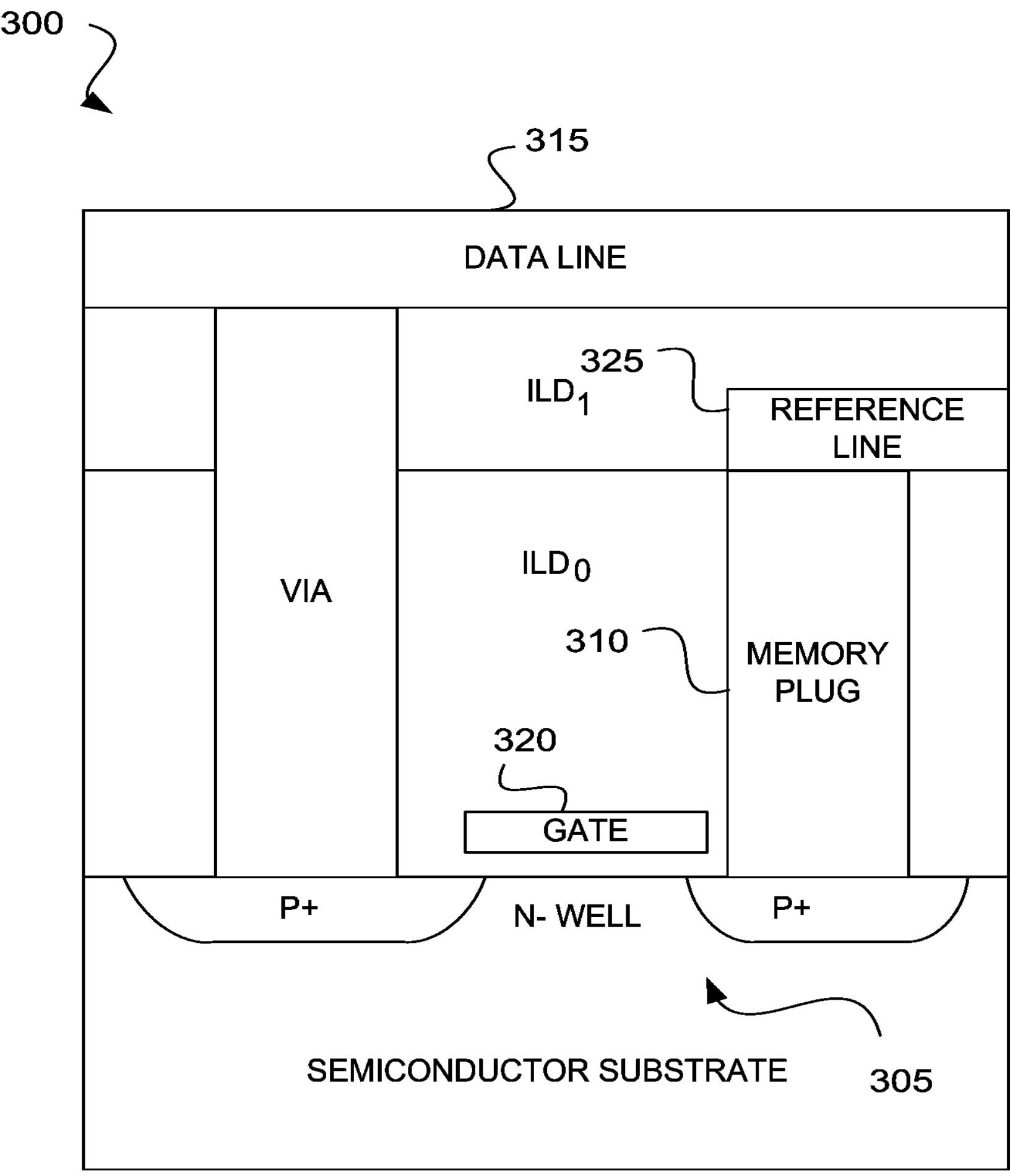
300
315
DATA LINE
325
ILD1
REFERENCE LINE
VIA
ILD0
310
MEMORY PLUG
320
GATE
P+
N- WELL
P+
SEMICONDUCTOR SUBSTRATE
305

FIG. 3

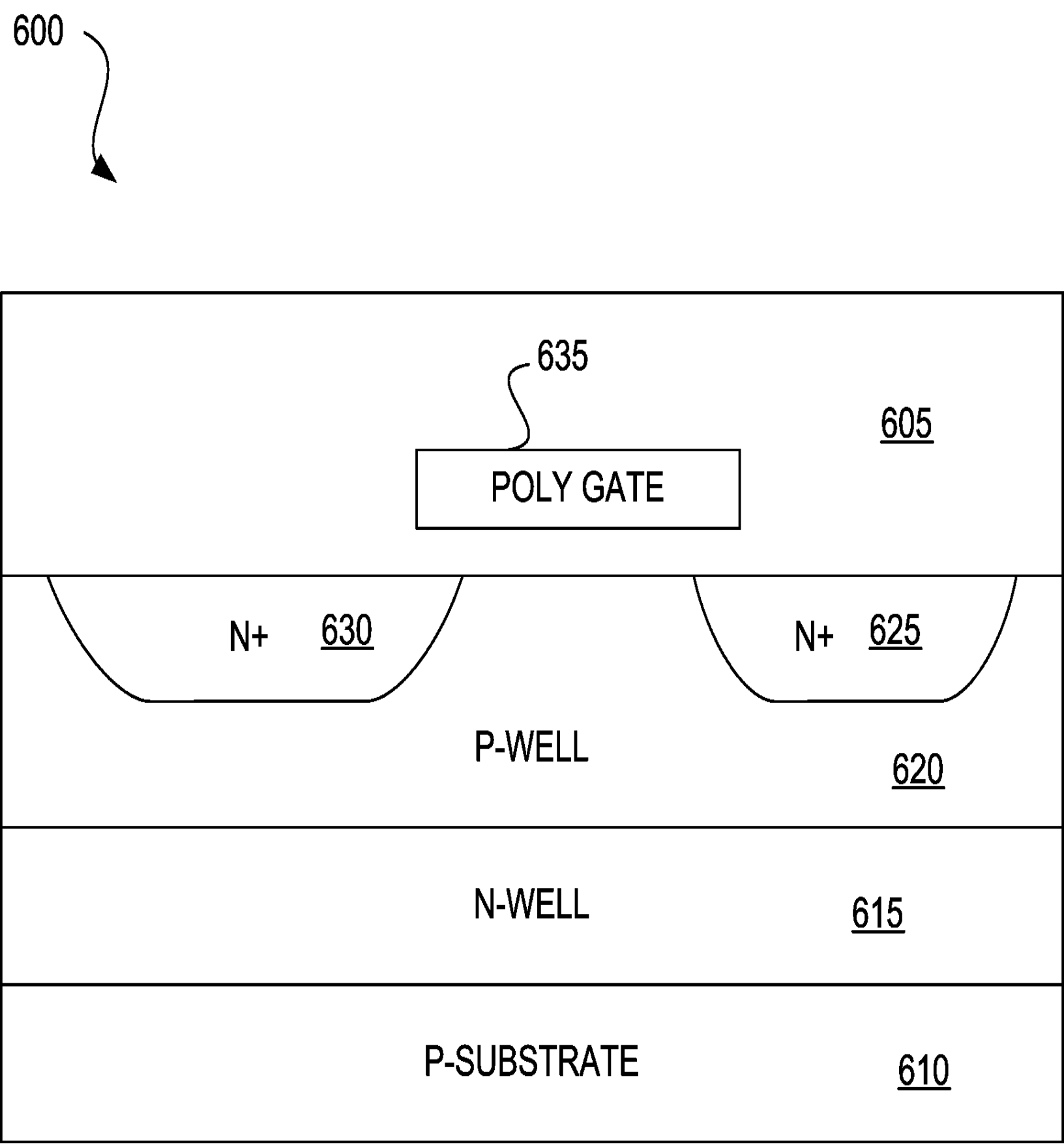
600
635
605
POLY GATE
N+ 630
N+ 625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 4

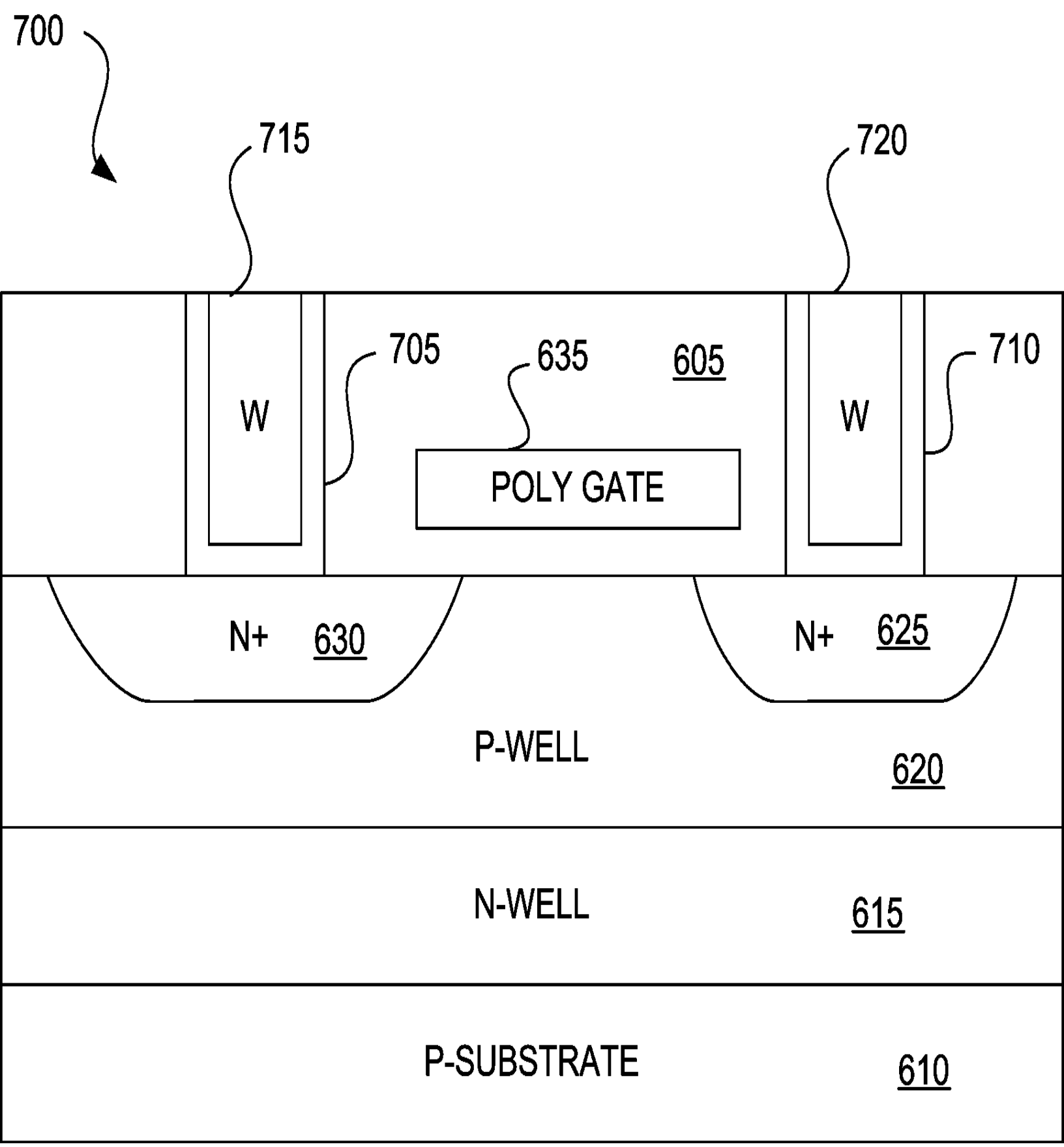
700
715
720
W
705
635
605
710
W
POLY GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 5

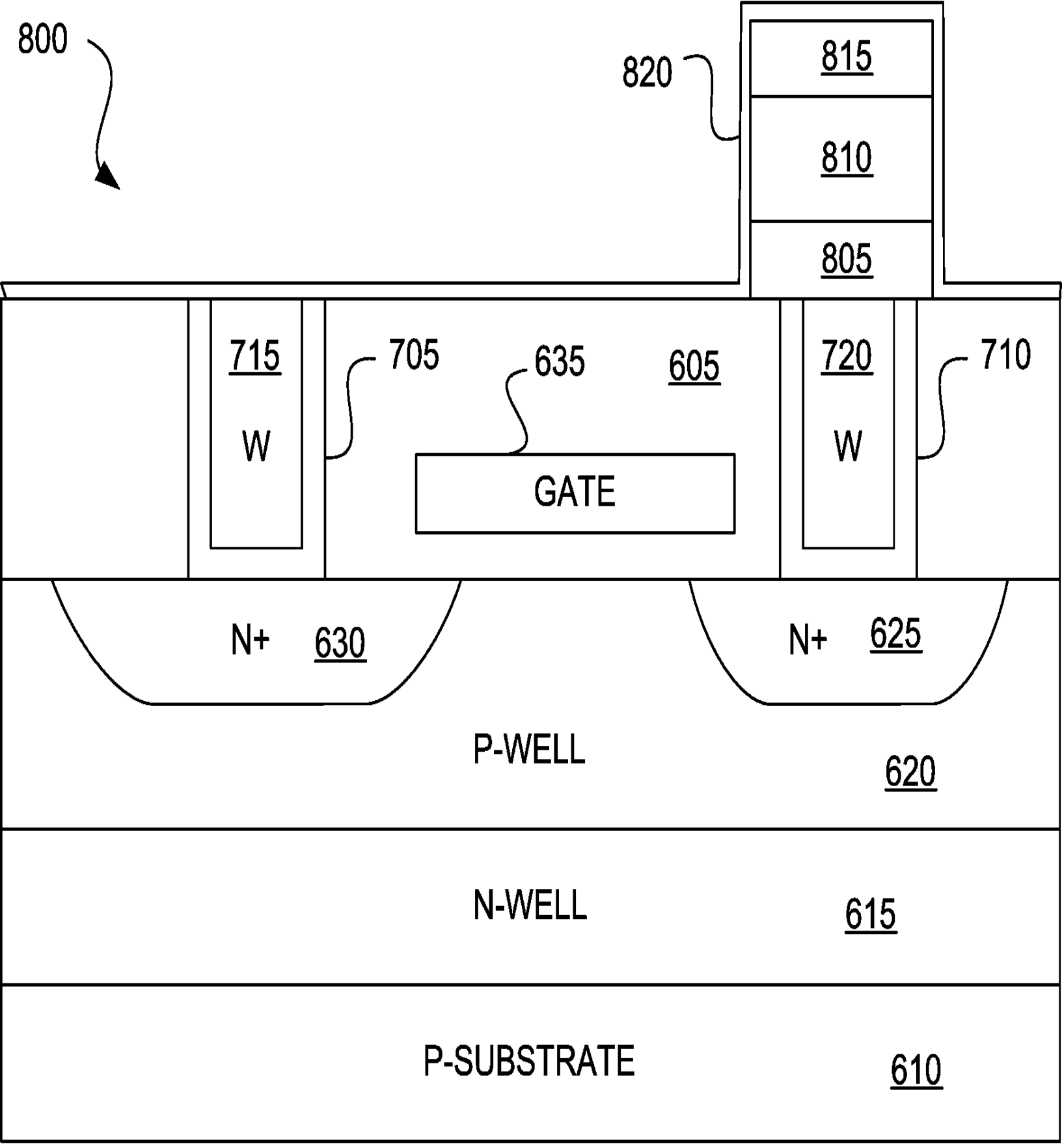
800
820
815
810
805
715
W
705
635
605
720
W
710
GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 6

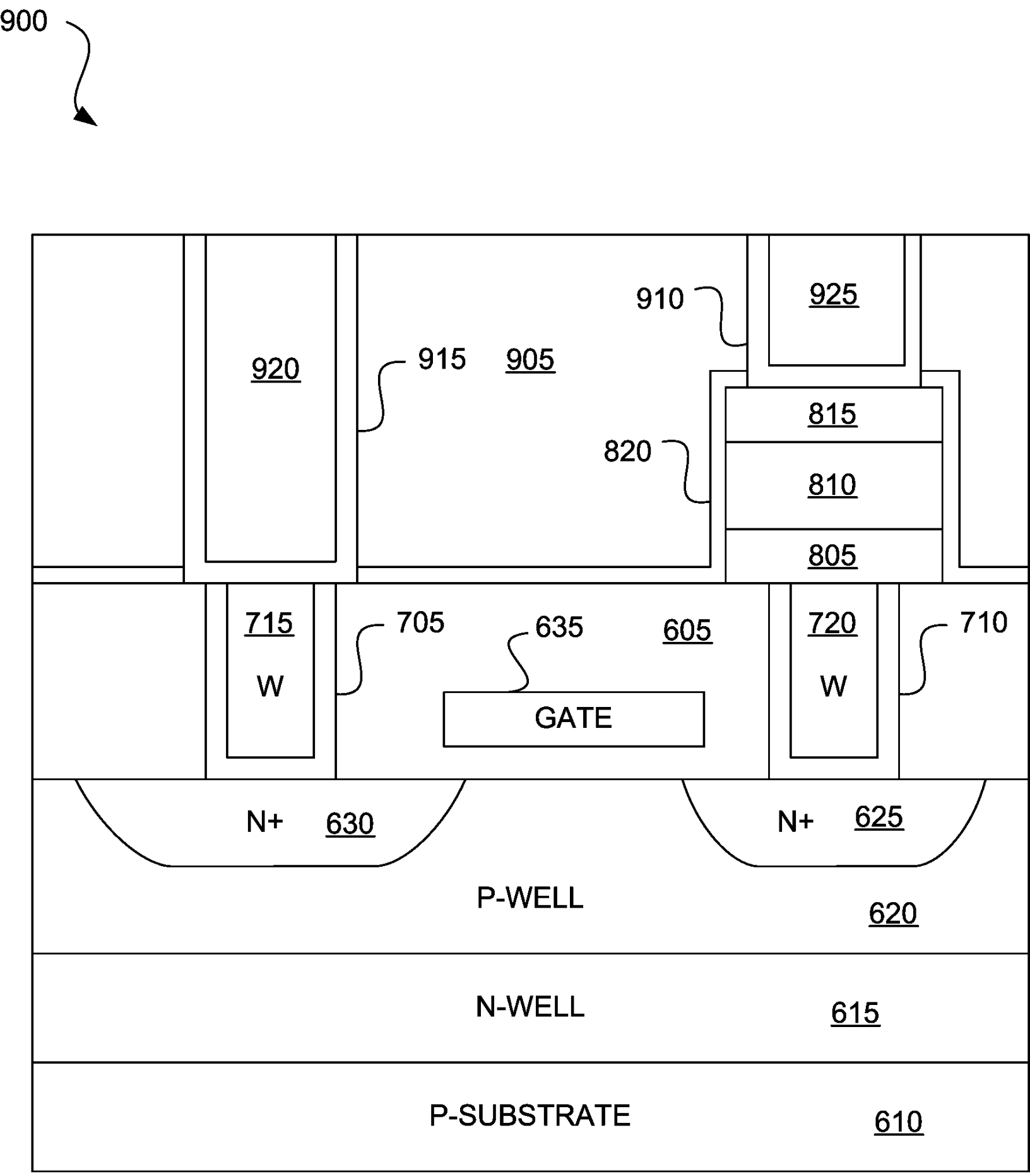
900
910
925
920
915
905
815
820
810
805
715
W
705
635
605
720
W
710
GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 7

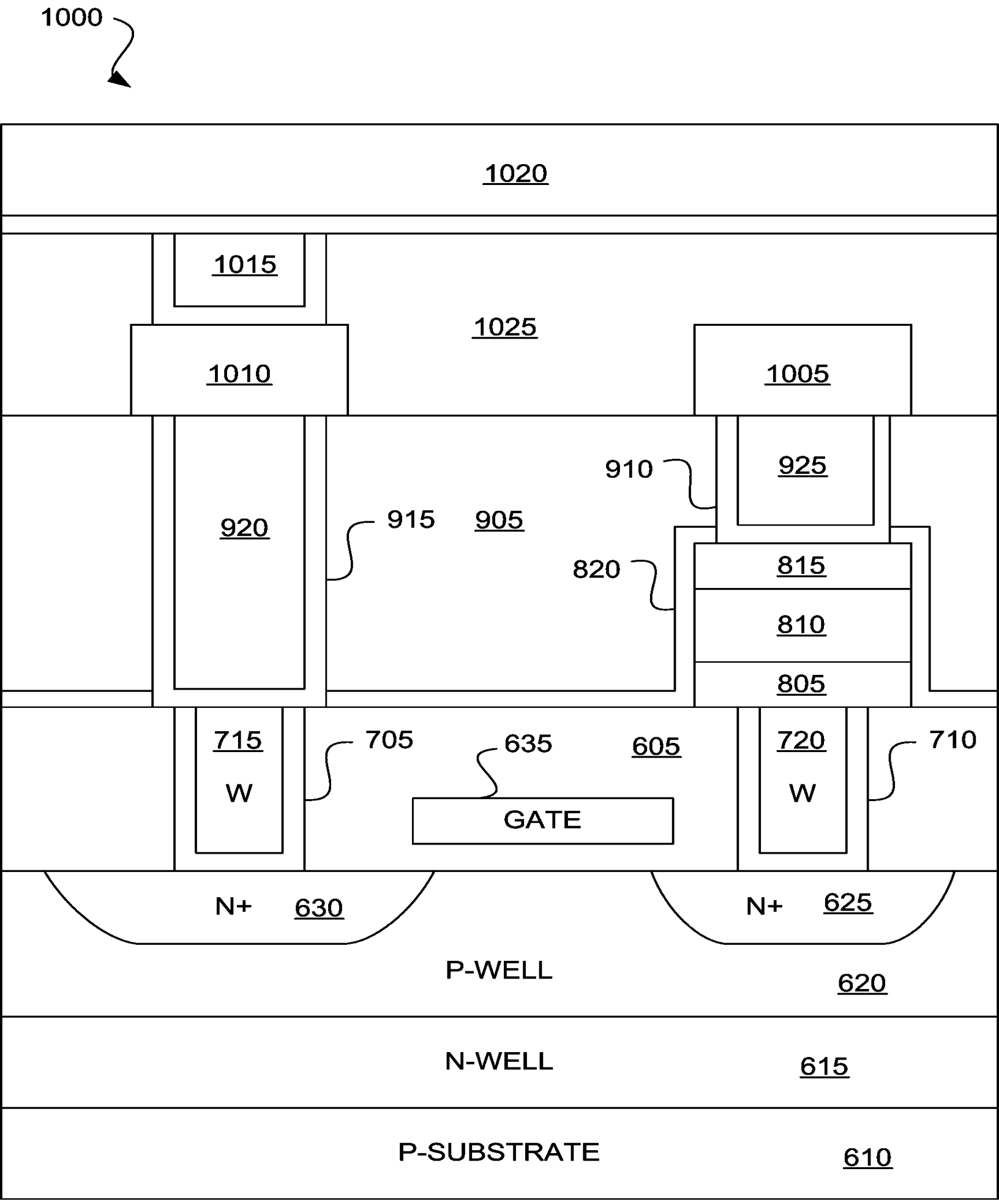
1000
1020
1015
1025
1010
1005
910
925
920
915
905
820
815
810
805
715
W
705
635
605
720
W
710
GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 8

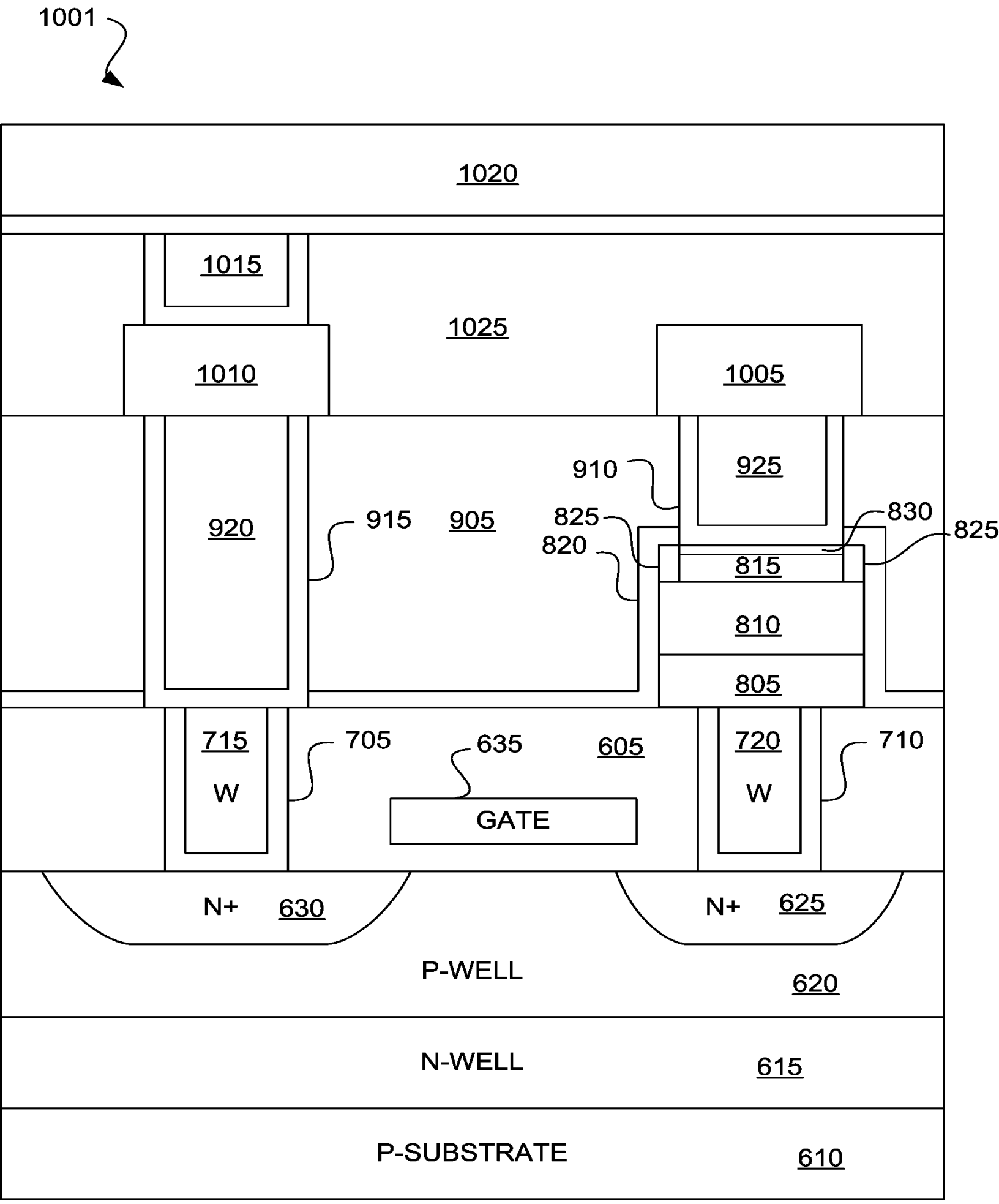
1001
1020
1015
1025
1010
1005
910
925
920
915
905
825
830
820
825
815
810
805
715
W
705
635
605
720
W
710
GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 9

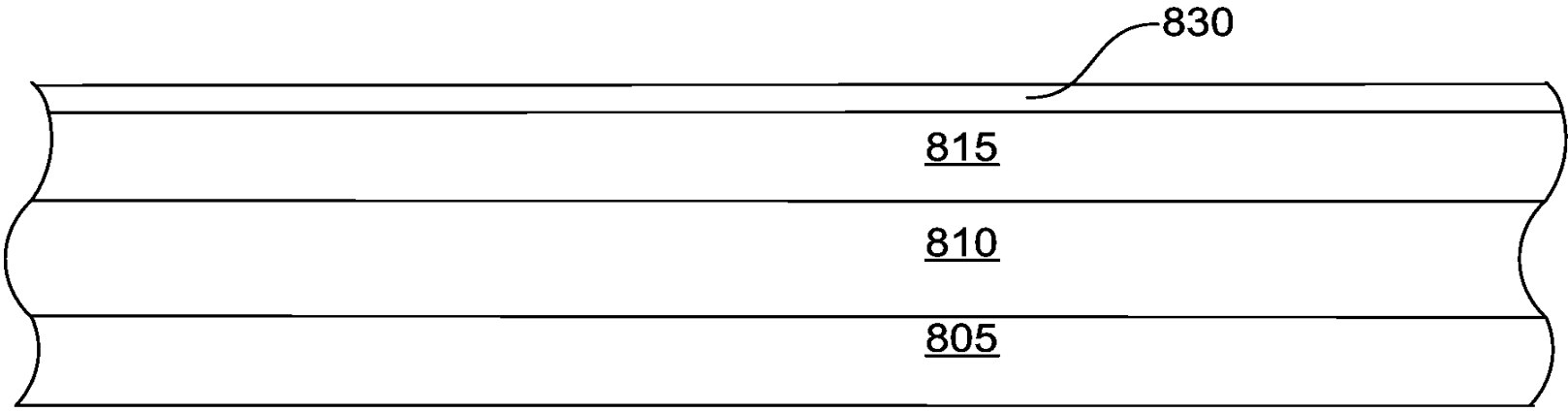


FIG. 10A

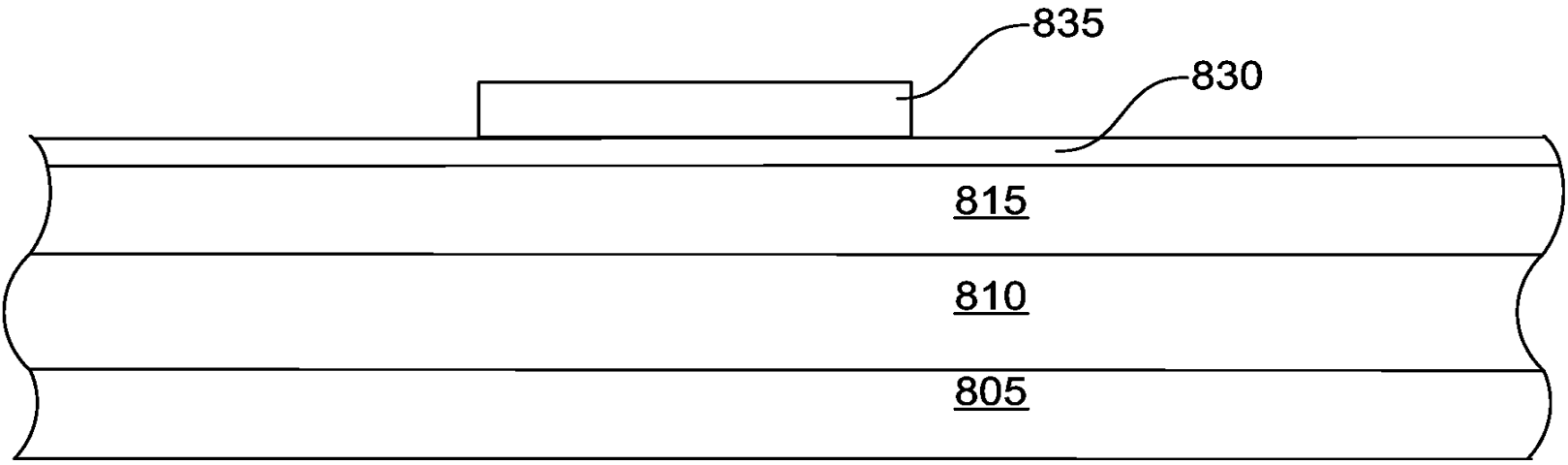


FIG. 10B

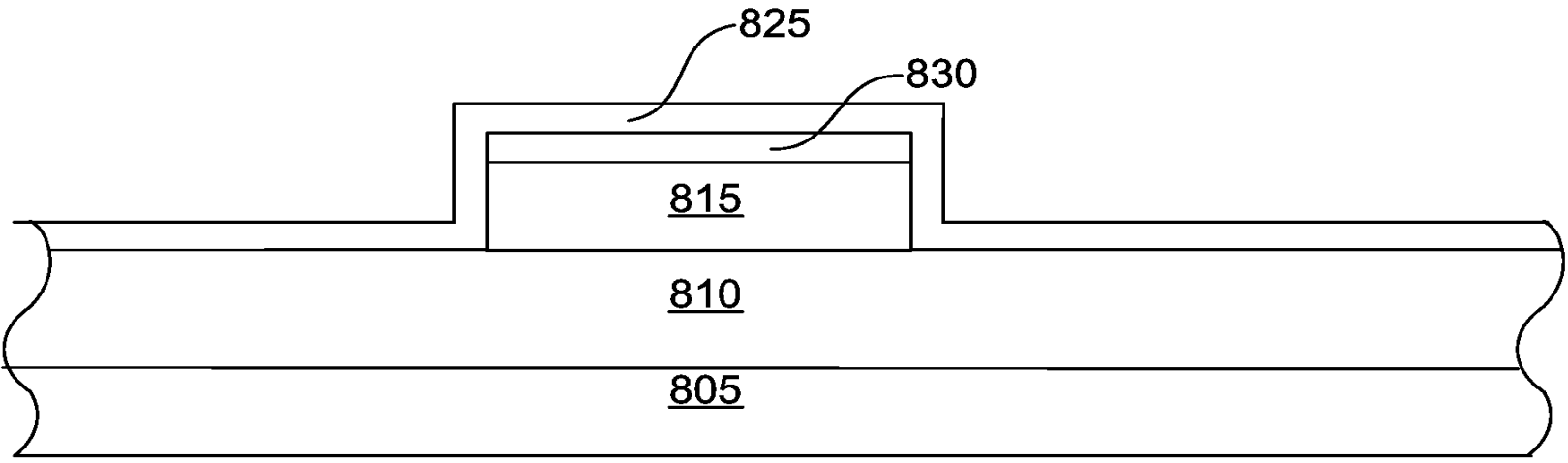


FIG. 10C

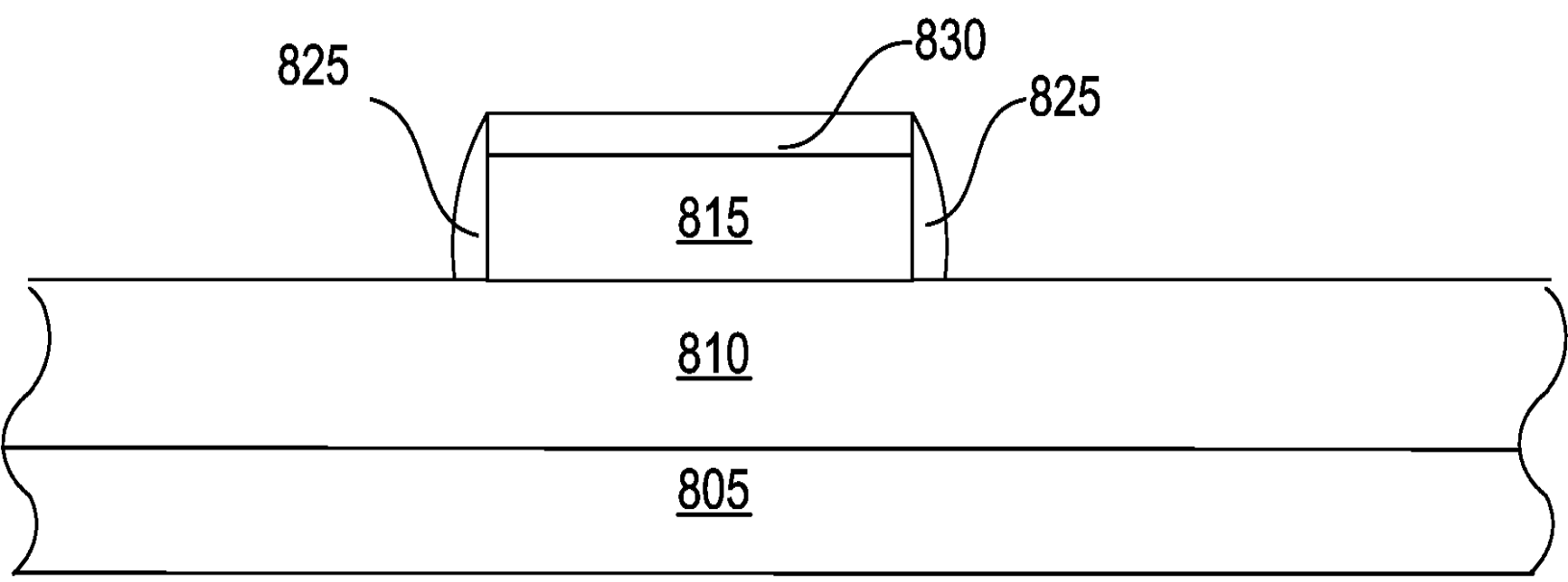


FIG. 10D

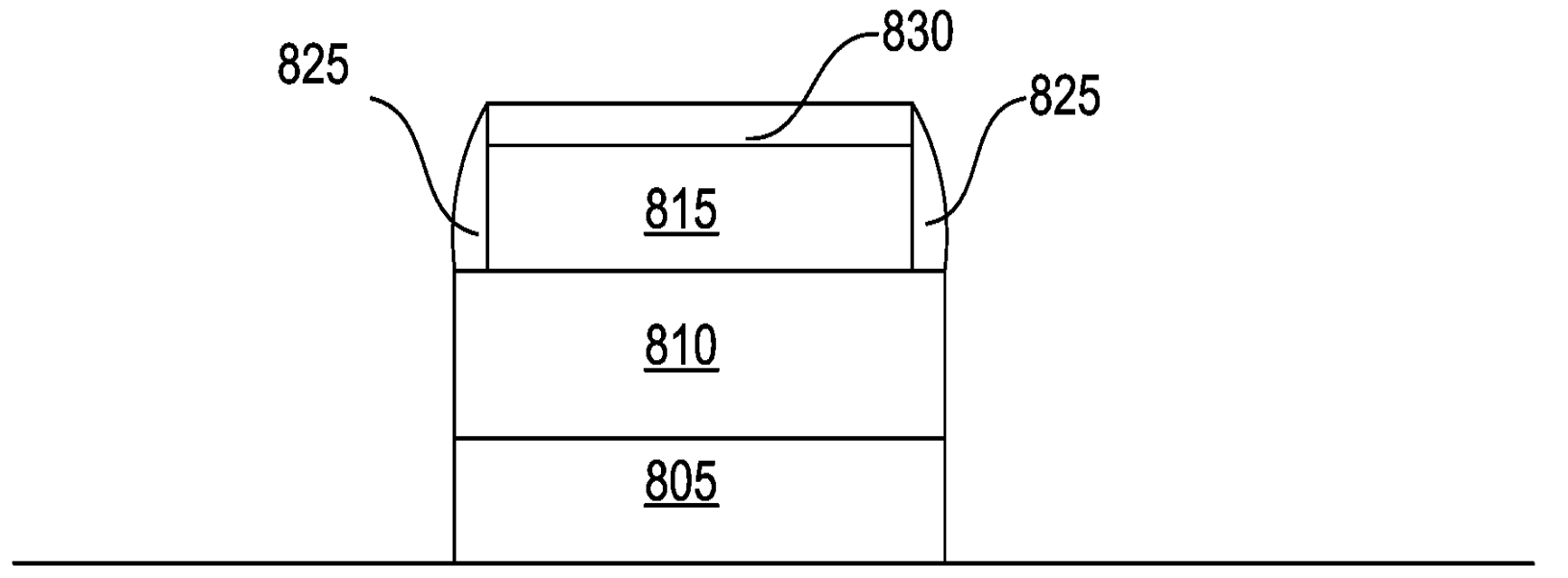


FIG. 10E

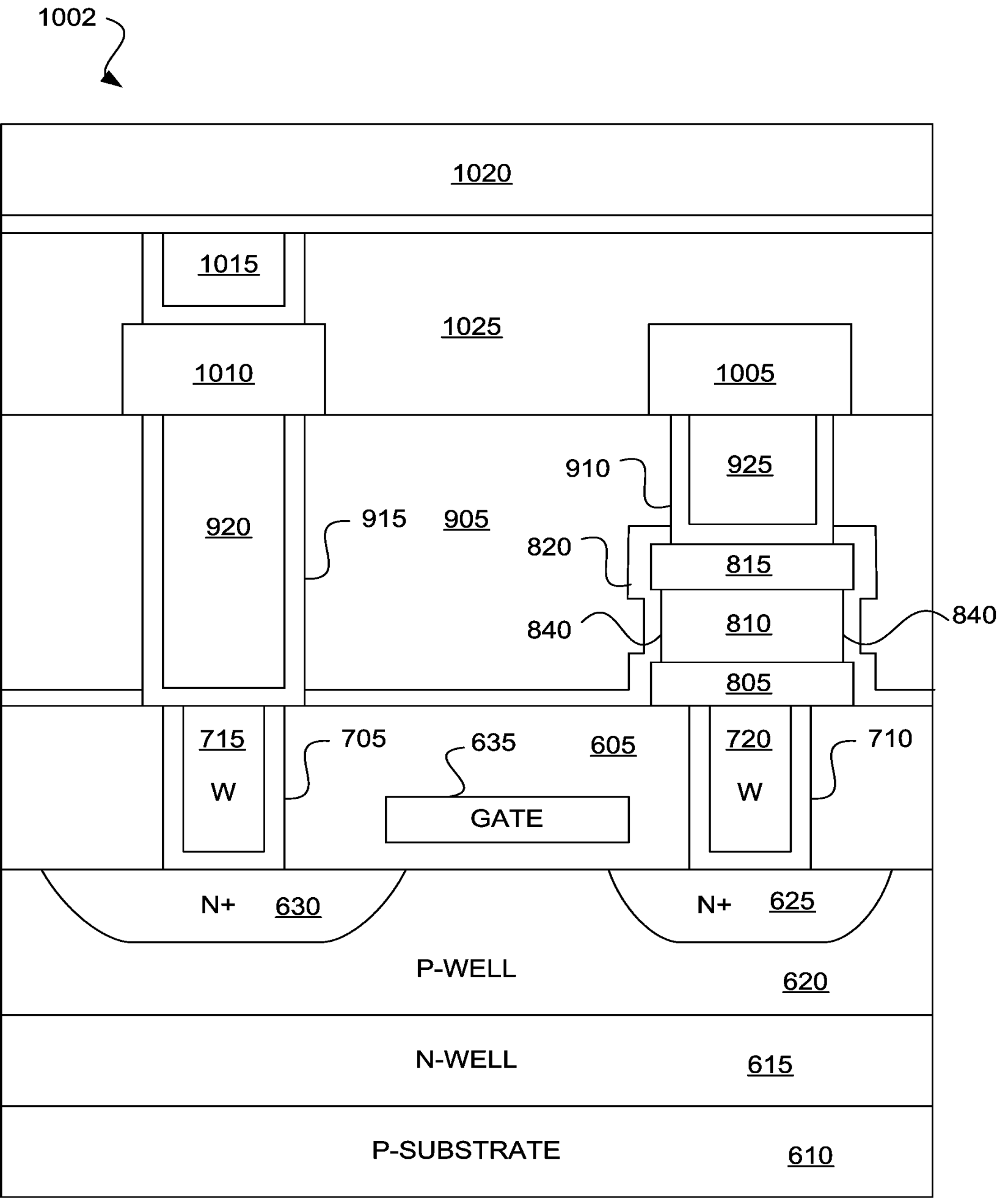
1002
1020
1015
1025
1010
1005
910
925
920
915
905
820
815
840
810
840
805
715
W
705
635
605
720
W
710
GATE
N+
630
N+
625
P-WELL
620
N-WELL
615
P-SUBSTRATE
610

FIG. 11